

Ultralow Distortion, 600 MHz Buffer

FEATURES

Excellent Gain Accuracy: 0.994 V/V Wide Bandwidth: 600 MHz Slew Rate: 2200 V/us **Ultralow Distortion:**

-73 dBc @ 20 MHz -91 dBc @ 2.3 MHz

Fast Settling Time: 8 ns to 0.02%

Low Noise: 2.0 nV/√Hz

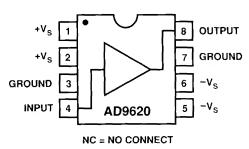
APPLICATIONS IF/Communications Impedance Transformations **Drives Flash ADCs** Line Driving

GENERAL DESCRIPTION

The AD9620 is a monolithic, unity gain buffer amplifier that sets new standards in gain accuracy, wide bandwidth and low distortion. Its large signal bandwidth, ultralow distortion over frequency, and drive capabilities of the AD9620 make this buffer an ideal driver for flash ADCs. Other applications which require increased current drive at unity voltage gain, such as cable driving, also benefit from the AD9620's performance.

In addition to innovative (patent pending) feedback architecture, special packaging techniques improve dynamic performance by minimizing the reactive effects associated with standard packages. The result is -73 dBc harmonic suppression at 20 MHz, and -91 dBc at 2.3 MHz. The AD9620 also outperforms other amplifiers, including its predecessor AD9630, in terms of smallsignal pulse response and dc linearity. These features make the AD9620 the premier driver for high speed, high resolution ADCs.

DIP CONFIGURATION



Available in side-brazed ceramic DIP packages, the "A" suffix unit is guaranteed for -40°C to +85°C operating temperatures; the "S" suffix device is guaranteed from -55°C to +125°C. AD9620 die are dc tested at +25°C.

*Patent(s) Pending.

AD9620 — SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50 \Omega$, $R_{LOAD} = 100 \Omega$)

			Test	AD9620AD		AD9620SD				
Parameter	Conditions	Temp	Level	1	Typ	Max	Min	Typ	Max	Units
Parameter DC SPECIFICATIONS Output Offset Voltage Offset Voltage TC Input Bias Current Bias Current TC Input Resistance Input Capacitance Gain Output Voltage Range Output Current (50 Ω Load) Output Impedance Power Supply Rejection Ratio DC Nonlinearity	Conditions $V_{OUT} = 2 \text{ V p-p}$ $At \text{ DC}$ $\Delta V_S = \pm 5\%$ $\pm 2 \text{ V Full Scale}$	Temp +25°C Full +25°C Full +25°C To T _{max} T _{min} +25°C Full Full Full +25°C Full	I IV I IV VI VI VI VI VI VI VI VI VI	-8 -25 -35 -150 400 190	±2 ±5 ±6	+8 +25 +35 +150	-8 25 35	±2 ±5 ±6 ±50 800	+8 +25 +35 +150	mV μV/°C μA nA/°C kΩ pF V/V V mA Ω dB %
FREQUENCY DOMAIN Bandwidth (-3 dB) Small Signal Small Signal Large Signal Large Signal Amplitude of Peaking Amplitude of Peaking Amplitude of Rolloff Group Delay Phase Nonlinearity 2nd Harmonic Distortion	$V_{OUT} = \le 0.7 \text{ V p-p}$ $V_{OUT} = \le 0.7 \text{ V p-p}$ $V_{OUT} = 4 \text{ V p-p}$ $V_{OUT} = 4 \text{ V p-p}$ $\le 150 \text{ MHz}$ $\le 150 \text{ MHz}$ $\le 150 \text{ MHz}$ DC to 150 MHz DC to 150 MHz 2 V p-p; 2.3 MHz 2 V p-p; 2.3 MHz 2 V p-p; 20 MHz 2 V p-p; 60 MHz 2 V p-p; 60 MHz 2 V p-p; 2.3 MHz 2 V p-p; 60 MHz 2 V p-p; 60 MHz 2 V p-p; 20 MHz 2 V p-p; 20 MHz 2 V p-p; 20 MHz	$T_{\min} \text{ to } +25^{\circ}\text{C}$ T_{\max} $T_{\min} \text{ to } +25^{\circ}\text{C}$ T_{\max} $T_{\min} \text{ to } +25^{\circ}\text{C}$ T_{\max} $Full$ $+25^{\circ}\text{C}$ $+25^{\circ}\text{C} \text{ to } T_{\max}$ $Full$ $+25$ T_{\min} $Full$ $+25$ T_{\min} $Full$ $Full$ $Full$ $Full$ $Full$ $Full$	II II IV IV II II II V V IV IV IV IV IV	320 260 60 45	600 80 0.8 1.5 0 0.75 1.4 -91 -81 -71 -69 -62 -94 -81 -60	1.5 2.2 0.3 -82 -73 -63 -60 -86 -71 -52	320 260 60 45	600 80 0.8 1.5 0 0.75 1.4 -91 -81 -71 -69 -62 -94 -81 -60	1.5 2.2 0.3 -82 -73 -63 -60 -86 -71 -52	MHz MHz MHz dB dB dB ns Degrees dBc
Spectral Input Noise Voltage Average Equivalent Integrated Output Noise Voltage	10 MHz 0.1 to 200 MHz	+25°C +25°C	V V		2.0			2.0		nV/\sqrt{Hz} μV
TIME DOMAIN Slew Rate Rise/Fall Time Overshoot Settling Time	$\begin{aligned} V_{\text{OUT}} &= 4 \text{ V Step} \\ V_{\text{OUT}} &= 1 \text{ V Step} \\ V_{\text{OUT}} &= 1 \text{ V Step} \\ V_{\text{OUT}} &= 4 \text{ V Step} \\ V_{\text{OUT}} &= 4 \text{ V Step} \\ V_{\text{OUT}} &= 2 \text{ V Step} \end{aligned}$	$+25^{\circ}$ C T_{\min} to $+25^{\circ}$ C T_{\max} T_{\min} to $+25^{\circ}$ C T_{\max} Full	IV IV IV IV IV	1500	2200 0.8 1.1 1.7 2.3 3	1.2 1.5 2.5 3.4 12	1500	2200 0.8 1.1 1.7 2.3 3	1.2 1.5 2.5 3.4 12	V/µs ns ns ns ns %
To 0.1% To 0.02% Differential Gain Differential Phase	$V_{\rm OUT} = 2 \text{ V Step}$ $V_{\rm OUT} = 2 \text{ V Step}$ 4.4 MHz 4.4 MHz	Full Full +25°C +25°C	IV IV V		6 8 0.02 0.02	10 16		6 8 0.02 0.02	10 16	ns ns % Degrees

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Parameter	Conditions	Temp	Test Level	 D9620 <i>i</i> Typ	AD Max	A Min	1D9620 Typ	SD Max	Units
POWER SUPPLY REQUIREM	ENTS								
Quiescent Current									
$+I_S$	$+V_S = +5 V$	Full	VI	40	48		40	48	mA
$-I_S$	$-V_S = -5 V$	Full	VI	40	48		40	48	mA

NOTES

Specifications subject to change without notice.

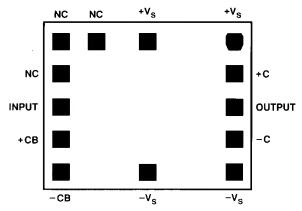
EXPLANATION OF TEST LEVELS

Test Level

- I 100% production tested.
- II 100% production tested at +25°C, and sample tested at specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI All devices are 100% production tested at +25°C.
 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

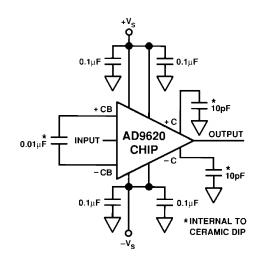
AD9620 DIE LAYOUT

 $60 \; (length) \times 50 \; (width) \times 15 \; (height) \; mils$



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option		
AD9620AD	−40°C to +85°C	8-Pin DIP	D-8		
AD9620SD	−55°C to +125°C	8-Pin DIP	D-8		
AD9620 Chips	+25°C	Dice			



AD9620 Bonding Diagram

THEORY OF OPERATION

The AD9620 is a wide bandwidth, unity gain buffer amplifier that utilizes innovative (patent pending) voltage feedback architecture. Large loop gain and high slew rate significantly improve dc linearity and large signal bandwidth when compared with that achieved with more conventional designs.

Its large-signal bandwidth compares favorably with competitive devices of open-loop design without their limitations. Open-loop devices often sacrifice dc linearity and introduce frequency distortion when driving low load impedances; the AD9620 does not. Its design yields low distortion products that are relatively constant for any resistive load greater than 50 ohms.

The AD9620 will satisfy any high performance analog signal processing application requiring isolation or current boosting between the signal source and load. Its combination of high input resistance and low capacitance, dc precision, and exceptional dynamic characteristics sets a new standard in performance that has no equal.

Excessive peaking may occur when using the AD9620 to directly drive loads with more than 3 pF of capacitance. To prevent this, a small value of resistance (R_s) should be placed in series with

REV. A -3-

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²Output is short-circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

 $^{^3}$ Typical side-brazed thermal impedances (part soldered onto board): $\theta_{JA} = 110^{\circ}$ C/W; $\theta_{JC} = 20^{\circ}$ C/W.

⁴External capacitor of AD9620 is attached with 62 Sn/36 Pb/2 Ag solder. Board attachment temperatures should be reviewed to insure the capacitor does not reflow during board mounting.

AD9620

the buffer output. The following figure shows various values of R_s as a function of capacitive load.

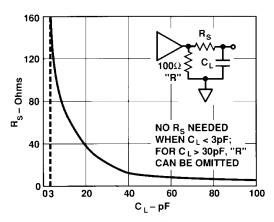


Figure 1. Recommended R_S vs. C₁

When the recommended series resistor is used, the AD9620 will have optimum frequency response, as shown in Figure 2.

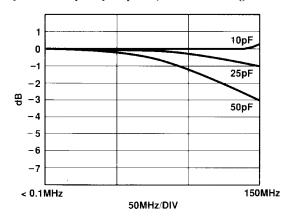


Figure 2. Frequency Response vs. C_L with Recommended R_S

Capacitive loads up to 50 pF can be driven with minimal degradation in pulse response with $R_{\rm S}$ equal to approximately 12 ohms

The output stage has short-circuit protection to ground, but average load currents greater than 70 mA may reduce device reliability. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is flowing. This ensures that output clipping will not occur during high slew conditions when driving capacitive loads.

LAYOUT CONSIDERATIONS

Although the AD9620AD/SD is housed in a specially designed package with built-in decoupling capacitors, the layout of the circuit containing the buffer requires careful attention. Without it, dynamic performance may be less than desired.

Optimum performance depends on connecting all of the supply pins and ground pins of the AD9620. If they are not connected, the inherent benefits of the buffer's special package will not be realized.

A two-ounce copper ground plane on the component side of the board is recommended. It should cover as much of the board as possible with appropriate openings for supply decoupling capacitors and for load and source resistors.

Settling time and ac performance will be optimized with surface mount 0.1 μF supply decoupling capacitors. These should be located within 50 mils of their corresponding device pins, with the opposite side of the capacitor soldered directly to the ground plane.

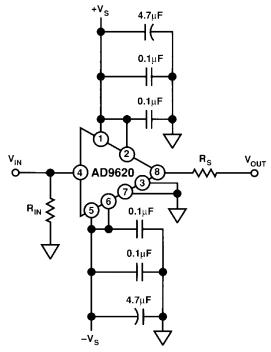


Figure 3. AD9620 Application Circuit (Ceramic DIP)

If surface mount capacitors cannot be used, radial lead ceramic capacitors with lead lengths less than 30 mils are recommended. Low frequency power supply decoupling is also necessary and can be accomplished with 4.7 μF tantalum capacitors mounted within 0.5 inch of the voltage supply pins. The interaction of the series inductance of the tantalum capacitor with the 0.1 μF decoupling capacitor and the supply leads may cause high frequency oscillations at the output. These can be eliminated with a ferrite bead mounted between the tantalum and ceramic capacitors.

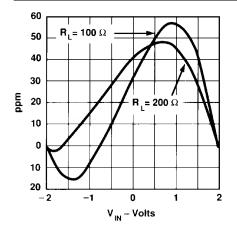
Connections to the AD9620 should be as short as possible. If either the source circuit or the driven circuit is further than one inch from the buffer, the printed circuit board (PCB) line impedances should be matched to the buffer input and output resistances. Basic microstrip techniques should be observed. The input termination resistor ($R_{\rm IN}$) and $R_{\rm S}$ should both be connected as close to the AD9620 as possible.

Its performance characteristics allow the AD9620 to drive terminated cables directly without the use of an output termination resistor for many applications. When used, termination resistors ($R_{\rm S}$ and $R_{\rm IN}$) can be either carbon composition or microwave types. When matching characteristic impedances, precision microwave resistors with tolerance of 1% or better are recommended.

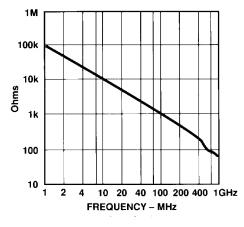
The AD9620 should be soldered directly to the PCB with minimum vertical clearance. The use of zero-insertion sockets is discouraged because of their high pin reactances. Use of this type socket will result in peaking and possibly induce oscillation. If sockets must be used for test or prototyping purposes, individual pin sockets such as the AMP 6-330808 series are recommended.

-4- REV. A

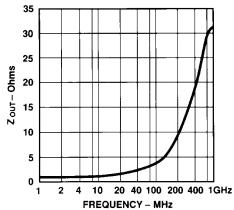
Typical Performance Curves—AD9620



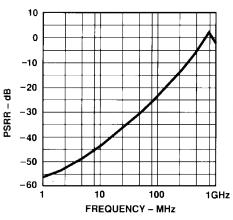
Endpoint DC Linearity Error



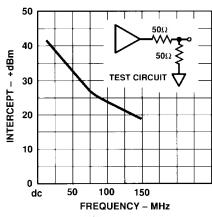
Input Impedance



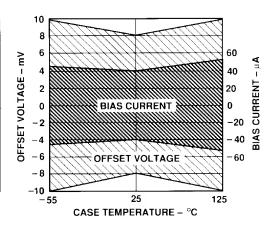
Output Impedance



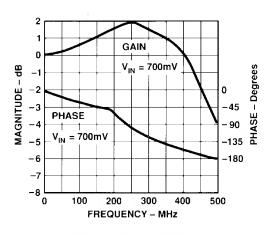
PSRR vs. Frequency



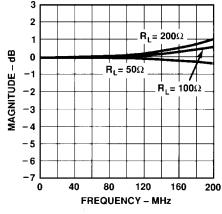
Two-Tone Intermodulation Distortion



Offset Voltage and Bias Current vs. Temperature (Worst Case)

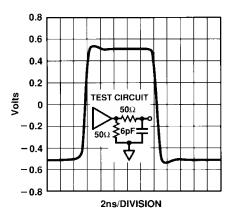


Forward Gain and Phase



Frequency Response vs. R_{LOAD}

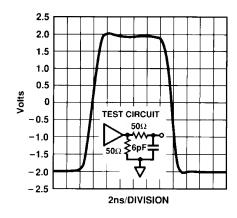
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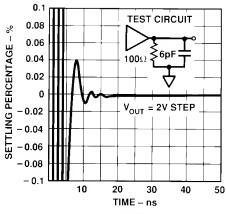


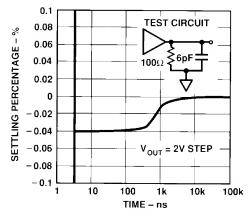
Small-Signal Pulse Response

REV. A

AD9620



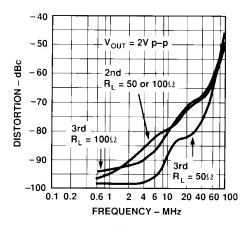


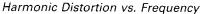


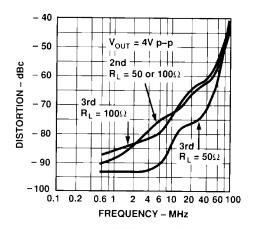
Large-Signal Pulse Response

Short-Term Settling Time

Long-Term Settling Time





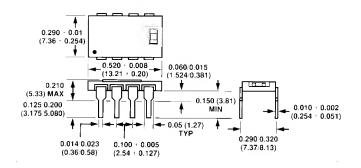


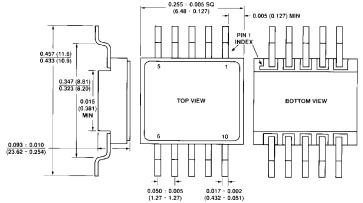
Harmonic Distortion vs. Frequency

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Suffixes AD and SD





NOTE: CONTACT FACTORY FOR INFORMATION ABOUT THIS AND OTHER PACKAGES FOR THE AD9620 BUFFER AMPLIFIER.